REMARKS

Reconsideration of the rejection of all of claims 13, 15-23 and 25-41 in the present application under 35 U.S.C. §103(a) is requested in light of the amendments being made to the claims and these Remarks. Some of the claim amendments are in response to the Office Action but others are being made to correct formal matters in the claims that were noted upon their further review, and yet others eliminate unnecessary limitations.

The claims are grouped for the purpose of this discussion according to the different combinations of prior art references used to reject them.

Claims 13, 15-18 and 37-41

This group includes independent claims 13 and 37. These claims have been rejected over a combination of patents nos. 6,011,725 ("Eitan") and 5,440,505 ("Fazio"). A third reference, a 1981 article in the *Journal de Physique* ("DiMaria"), has additionally been combined with these two references in rejecting dependent claims 16 and 39 of this group.

This rejection is traversed primarily on the ground that no reason appears in either of the cited Eitan or Fazio patent references for combining their teachings in the manner described by the Office Action to be necessary to meet the terms of the claims. Further, the Eitan patent expressly teaches away from using more than two programmable charge levels (herein "multi-state") in any one dielectric region.

In the Background (Eitan col. 3, ln. 57 – col. 5, ln. 2), a significant amount of space is devoted to advocate many disadvantages of multi-state operation of the type described by the Fazio patent. Programming and reading are said to be slow, the margins between the defined ranges are small, the threshold windows for the many states may change over time, higher voltages are required for operating the memory, and production yields are reduced. Additionally, Eitan emphasizes an advantage of being able to use two-state reading circuits (col. 23, lns 47 – 64) with his two-bit cell rather than the multi-state reading circuits required for prior art two-bit cells of the type described by Fazio.

The direction taken by Eitan to store more than one bit of data per memory cell is to store one bit of data in each of two spatially separated areas of a dielectric charge storage layer instead of operating with multiple charge levels as exemplified by Fazio. Even if one skilled in the art would have wanted to store more than two bits in each Eitan cell, something for which there is

no motivation shown in the cited references, the clear thrust of Eitan's disclosure is to avoid use of multi-state operation as described by Fazio. Eitan teaches use of either multi-state operation as described by Fazio, which is said to have its disadvantages, or binary (two-state) operation in each of two spatially separated charge storage regions, which is his invention.

It is therefore respectfully submitted that the cited Fazio patent would not have suggested to one skilled in the art that he or she should run contrary to the express teachings of Eitan by considering use of Fazio's multi-state operation in Eitan's device, particularly in the unique manner claimed where more than two charge level ranges at established at individual spatially separated dielectric charge storage regions. Eitan's spatially separated binary operation and Fazio's multi-state operation are described by Eitan as mutually exclusive alternatives.

An important additional point of novelty exists in independent claim 13, which has been limited to programming by the source side injection technique. Both Eitan and Fazio, on the other hand, describe the use of the hot-electron injection technique for programming. A discussion and definition of these different programming techniques is provided in the bottom paragraph of page 2 of the present application, with reference to the documents incorporated therein, particularly the book by Brown and Brewer, which have already been filed with Information Disclosure Statements. Use of the hot-electron injection technique results in charge being injected into the storage medium at positions adjacent the source and drain regions, which is what is done by Eitan.

Claim 13 has further been amended to recite that the charge storage regions are displaced from the source and drain regions, a result of programming by source side injection. In the present application, an example is shown in Figure 9, where charge storage regions 171 and 173, displaced from source and drain regions 152 and 153, result from source side injection. This clearly distinguishes Eitan, and Fazio provides nothing to suggest any modification in this regard. Eitan emphasizes that the charge storage regions must be adjacent the source and drain regions for his "reverse reading" technique to work. For example, in col. 23 lns. 17 – 28 of Eitan, the alignment of the charge storage regions with junctions of the source and drain regions is described to be "crucial." Thus, claiming the charge storage regions to be displaced from the source and drain regions as a result of programming by source side injection is a feature that is patentable over any combination of the teachings of Eitan and Fazio.

Claims 19-23 and 25-33

This group includes independent claims 19 and 23. These claims have been rejected over a combination of patent no. 5,278,439 ("Ma et al.") and Fazio. Additional references have been cited against dependent claims of this group: patent no. 5,889,303 ("Eckert") for claims 20 and 22; and a 1995 IEDM article ("Aritome") for claims 27, 32 and 33.

Independent claims 19 and 23 have been limited to use of the source-side injection programming technique and the resulting positions of the charge storage regions displaced from each other and from the source and drain regions within the storage dielectric. As pointed out in the Office Action, Fazio describes programming by hot-electron injection (col. 4, lns. 49 – 56), contrary to what is now being claimed. As discussed above, Eitan also programs by hot-electron injection. These claims are therefore patentable over any combination of the teachings of Eitan and Fazio since the claimed source side injection and the resulting positions of the charge storage regions are not suggested by either of these two references.

Dependent claim 20 adds a structural feature of the charge storage dielectric, namely that it extends completely across the memory cell between source and drain regions. In adding the Eckert patent to the combination of Eitan and Fazio for this feature, the Office Action mistakenly characterizes claim 20 as specifying the charge storage dielectric to extend between two control gates. Rather, the charge storage dielectric is claimed to extend between source and drain diffusions. The referenced floating gate 106 of Eckert is not shown in Figure 10 to extend between source and drain regions. But even if it did, it is not understood how this disclosure could have been combined with that of Eitan and Fazio to obtain the specific combination of claim 20.

Dependent claim 31 adds a structural configuration to the combination of claim 19 that is not even remotely suggested by the cited references. The first conductive gate (control line) and the second conductive gate (word line) are specified by claim 31 to be orthogonal with each other and contain dielectric charge storage regions under each. An example of this structure is shown in the embodiment of Figures 7 – 9 of the present application. Nothing like it appears in the cited references. Ma et al. has no floating gate under the word line 28, oriented perpendicularly with the control gates 20C and 22C (Ma et al. Figure 2A), for which a charge storage dielectric could be substituted.

Claims 34-36

Independent claim 34 and its dependent claims 35 and 36 have been rejected over patent no. 6,346,725 ("Ma 725") and Fazio. The Eckert patent additionally cited against dependent claim 35.

Similar to dependent claim 31 just discussed, independent claim 34 recites that a charge storage region exists in a charge storage dielectric positioned beneath the word line in addition to that under the orthogonally oriented control line. The Office Action alleges that the floating gate 60 in Figure 3 of the Ma 725 patent anticipates the claimed charge storage regions but this is not positioned between both the control gate and the substrate and the word line and the substrate. In case claim 34 was considered to be unclear in this regard, it has been amended to more positively recite the use of charge storage regions in dielectric material under both of the orthogonally oriented control and word lines.

The Ma 725 patent does not include any charge storage material (i.e., a floating gate) sandwiched between the word lines 710 (Figure 3L) and the substrate. Rather, the word line 710 extends between floating gates 60. So the alleged obviousness of substituting dielectric storage material for the floating gates of Ma 725 would not result in the claimed combination including a dielectric charge storage region under the word line as is claimed.

Because the feature of storing charge under both of the orthogonally oriented control and word lines is not suggested by any combination of the teachings of the Ma 725 and Fazio patents, claim 34 is being amended to remove the limitation to programming by hot-electron injection or source side injection that was inserted by the last Amendment.

Dependent claim 35 adds the feature that the dielectric material extends across the substrate between source and drain regions. The Eckert patent has been cited, along with Ma 725 and Fazio, to reject this claim. However, as expressed above with respect to claim 20, this combination does not anticipate all the features of the claim.

Information Disclosure Statements

It does not appear that a Supplemental Information Disclosure Statement Under 37 §1.97(c) with Fee, filed May 14, 2003 and citing 16 additional references, has yet been considered by the Examiner. Indeed, there is no reference of it in the USPTO PAIR record of the present application. Therefore, a copy is being filed herewith, with a duplicate of the cited

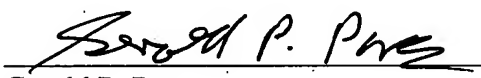
foreign patent reference, along with a copy of the USPTO return postcard receipt as evidence of the filing. If copies of any of the listed U.S. patent references are needed by the Examiner, please call the undersigned attorney so that they may be promptly provided.

A further Supplemental Information Disclosure Statement is being filed herewith, citing 3 additional references. Consideration of all the cited references and making them of record in the file of the present application are respectfully requested.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned attorney at 415-318-1163 would be appreciated.

Respectfully submitted,



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